

Fig. 1A

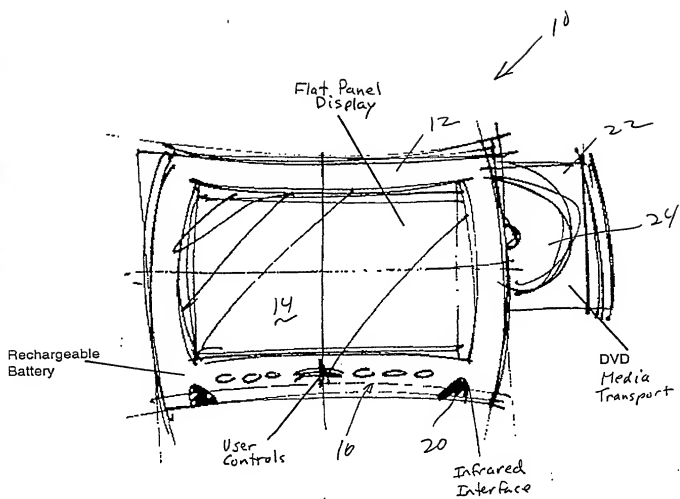


FIG. 2A

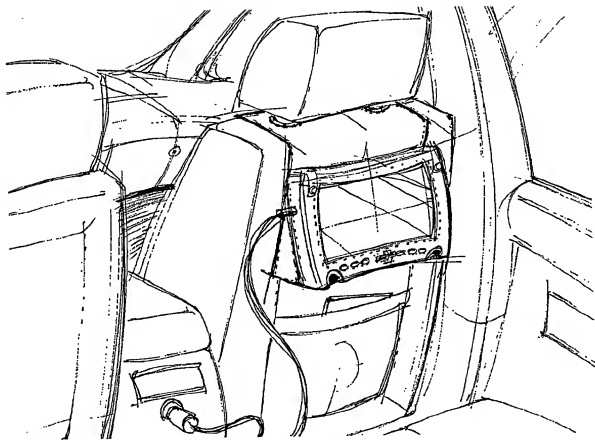


FIG. 2A



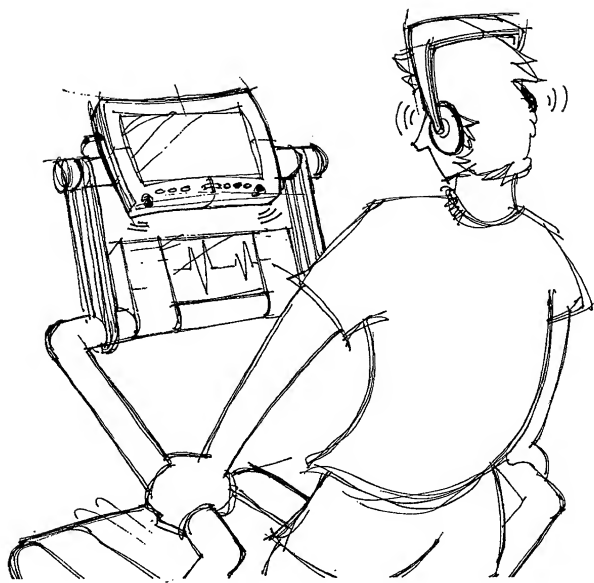


FIG. 2C

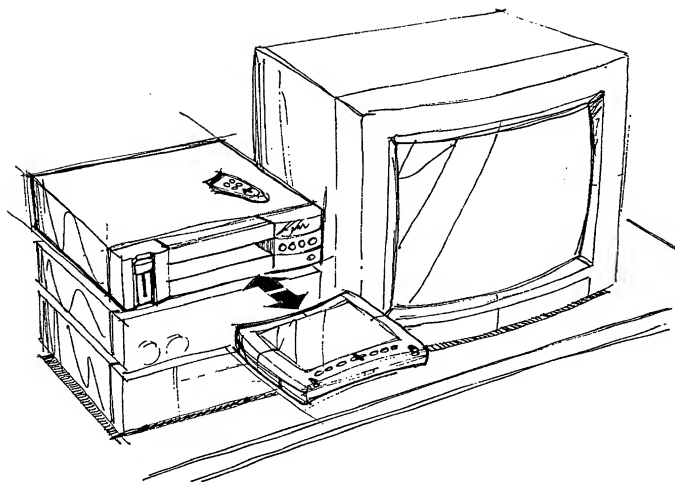


FIG. 2D

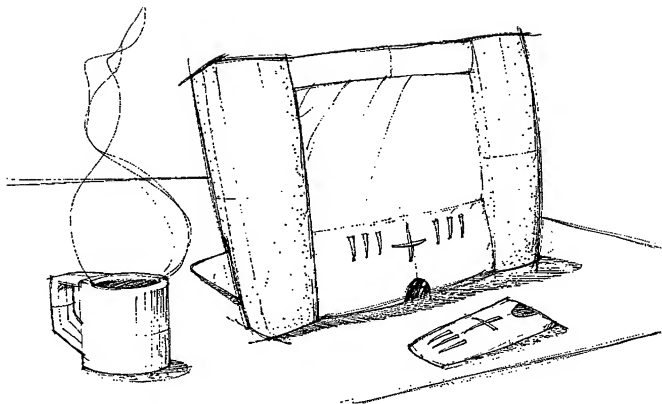


FIG. 2E

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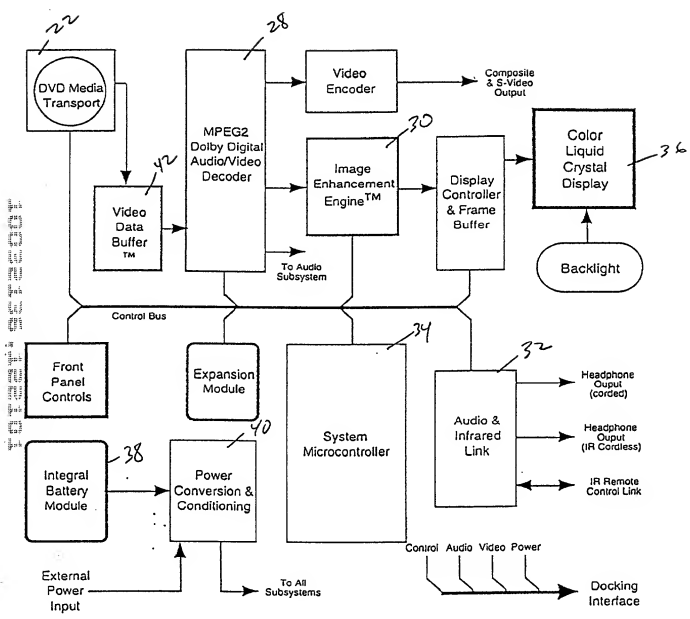


Fig. 3



30

50

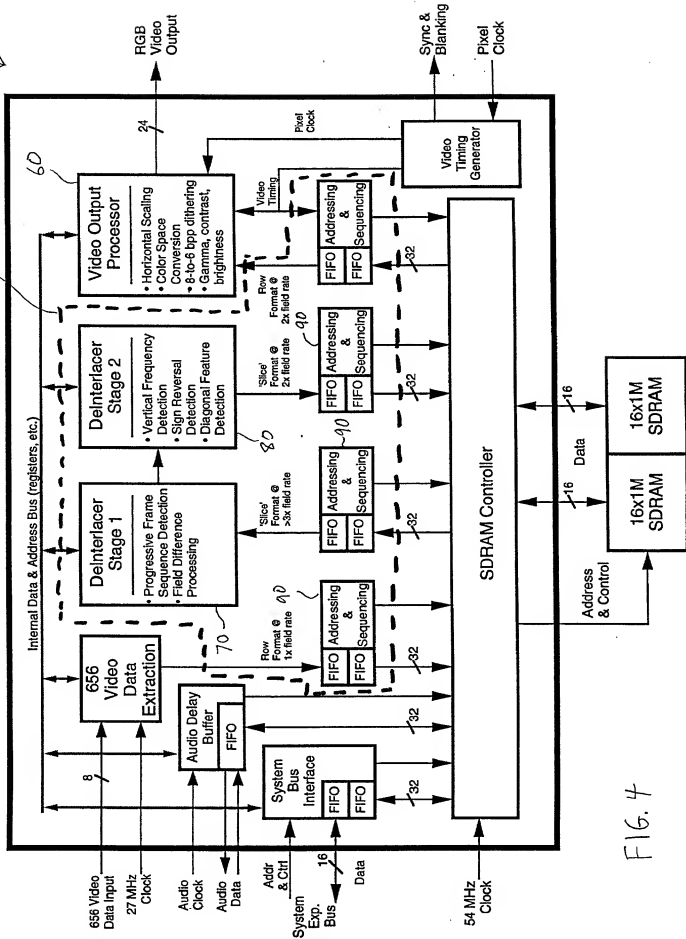


FIG. 4

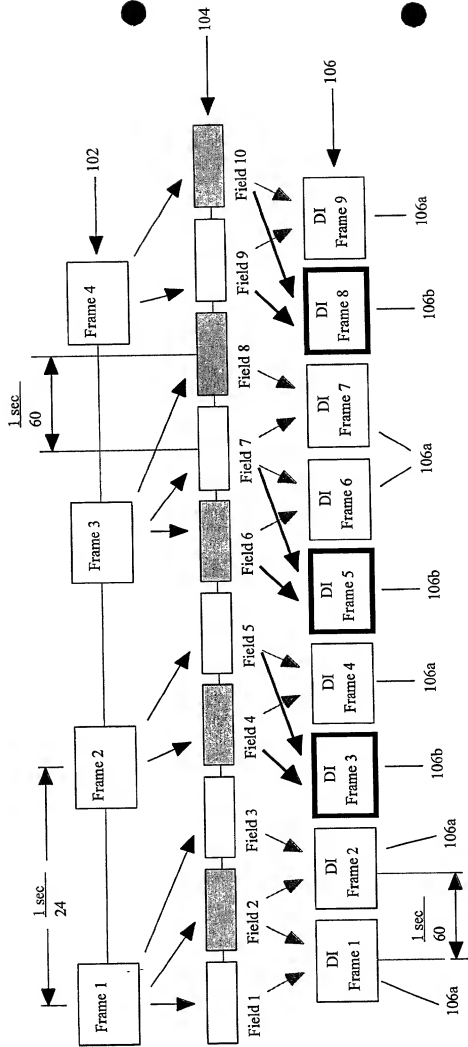


Figure 5

130

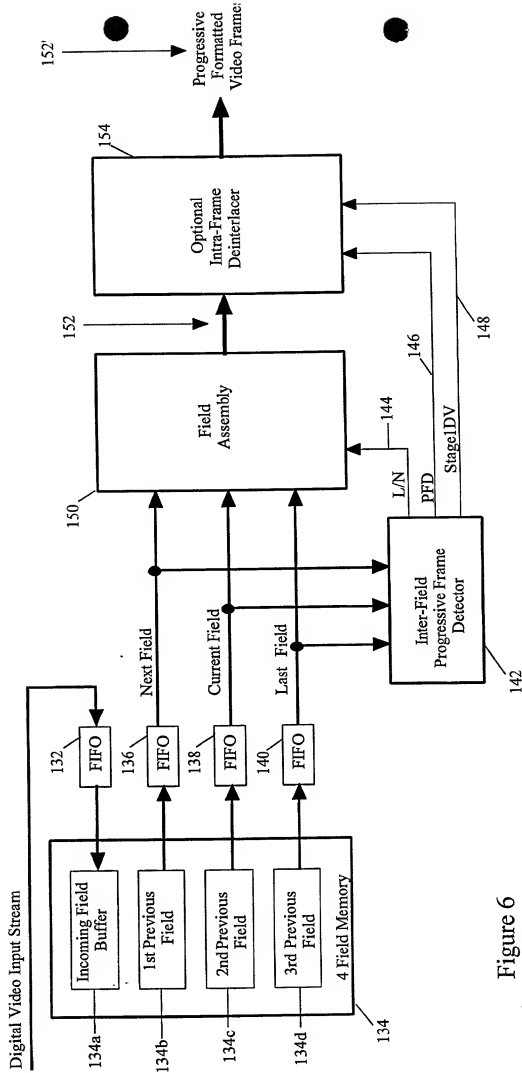


Figure 6

142 ↗

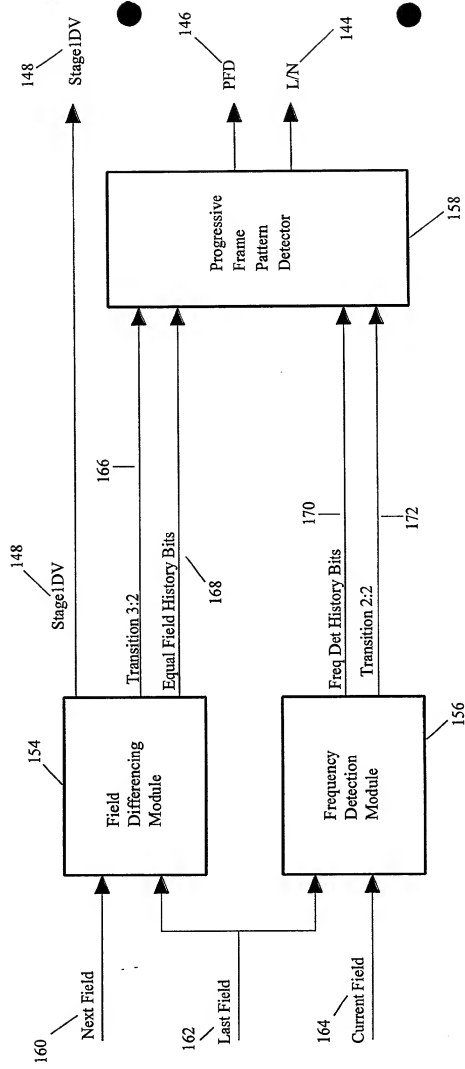


Figure 7

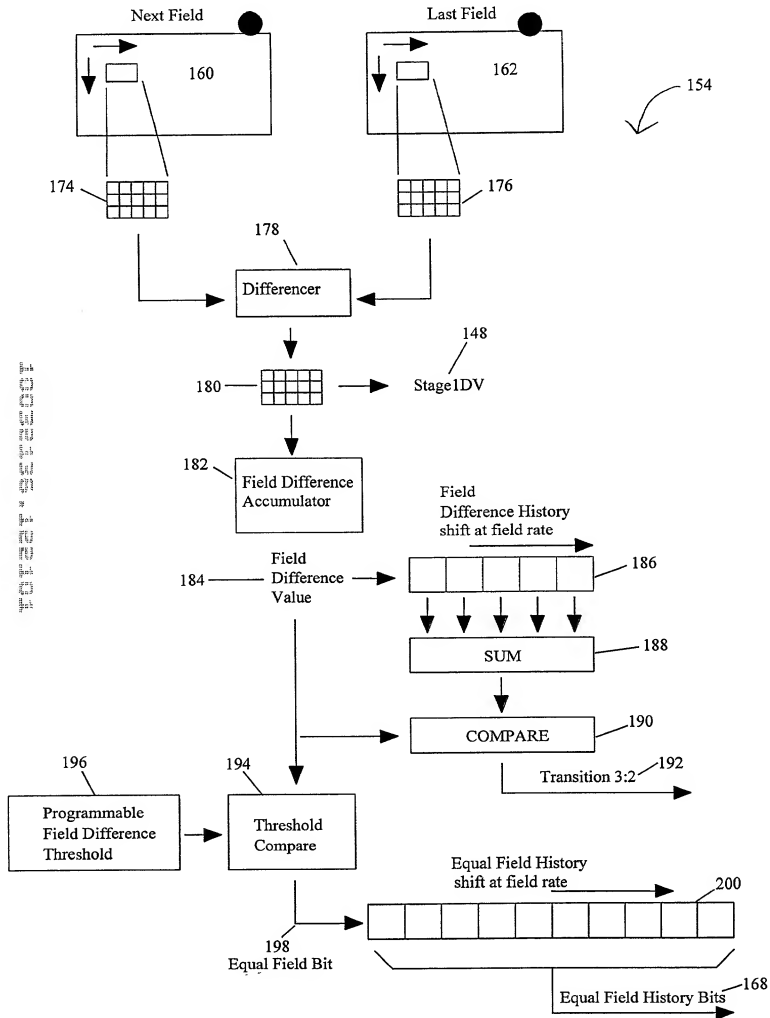


Figure 8

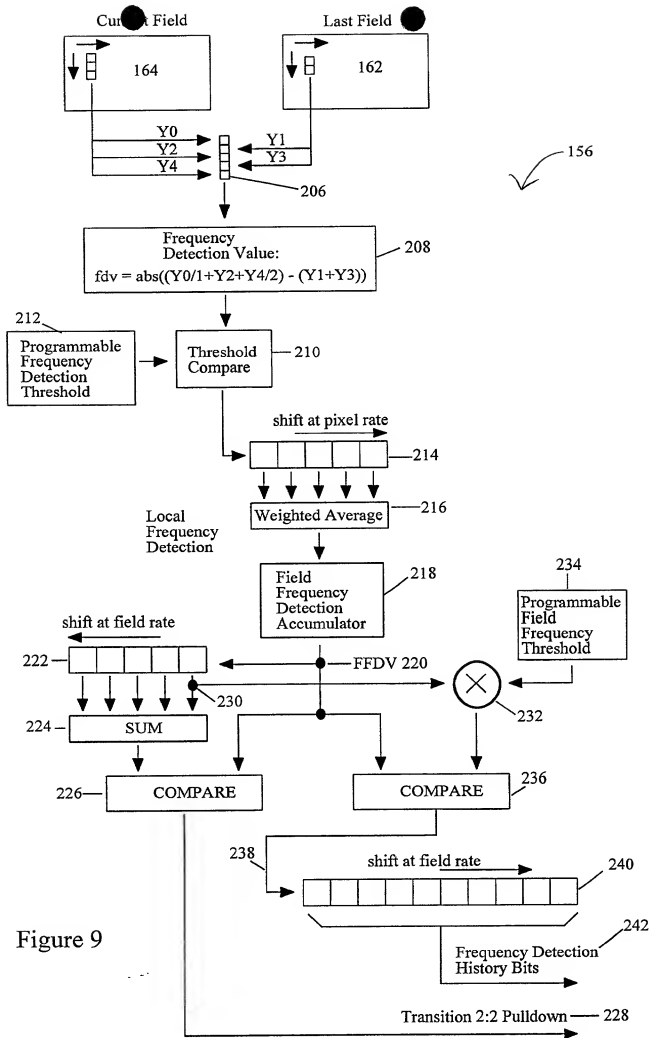


Figure 9

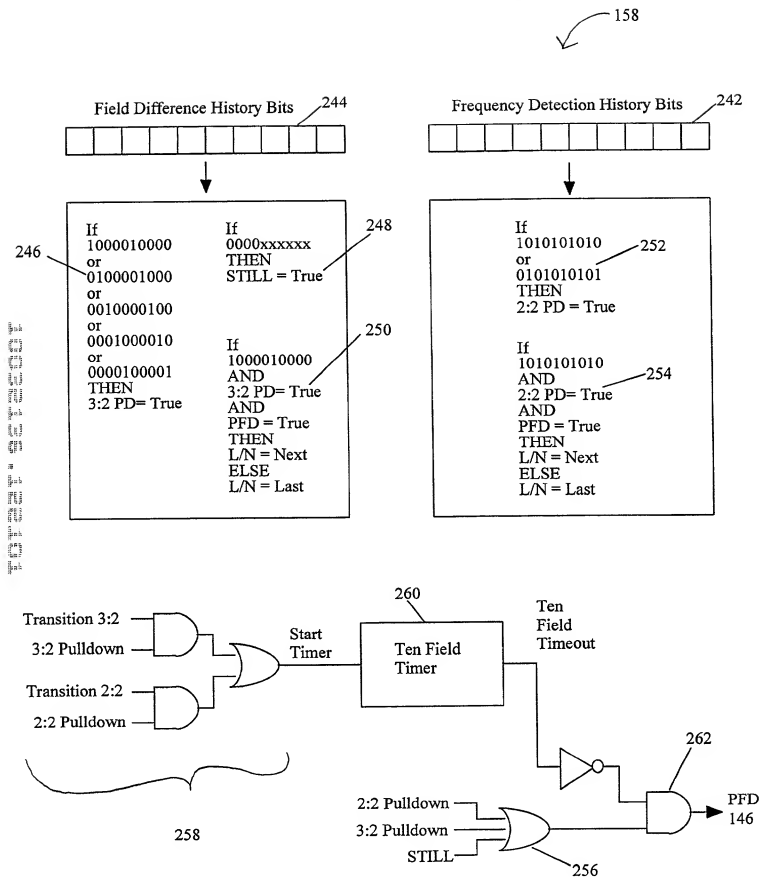


Figure 10

Figure 11

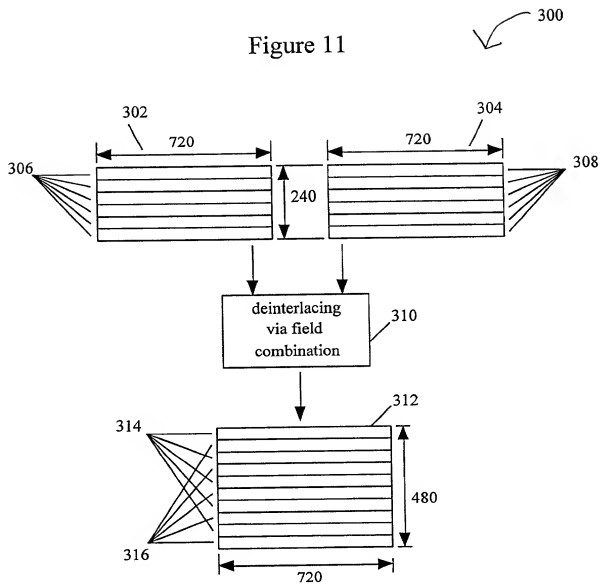
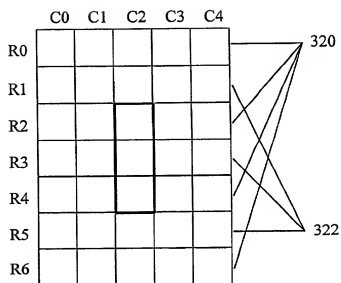
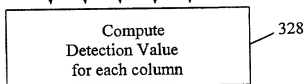
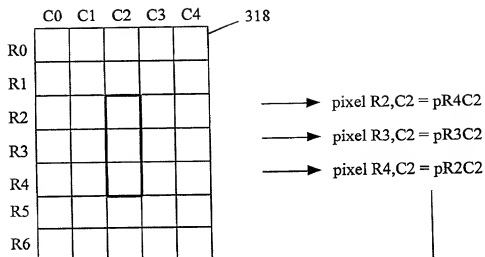




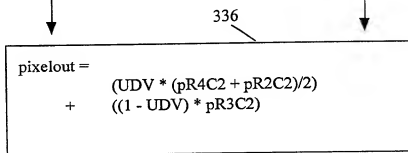
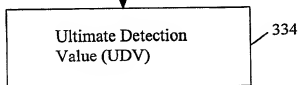
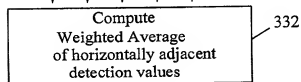
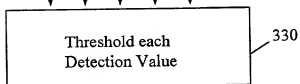
Figure 12

318



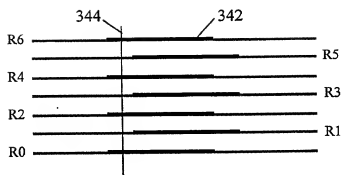
fd0 | fd1 | fd2 | fd3 | fd4



output pixel 338

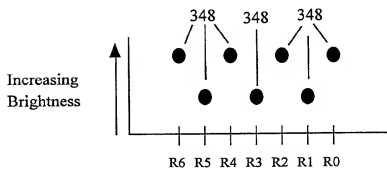
Figure 13

Figure 14A



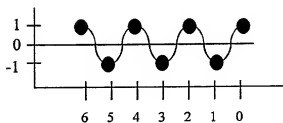
340

Figure 14B



346

Figure 14C



350

Figure 15

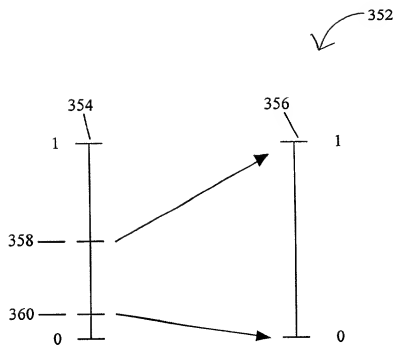


Figure 16

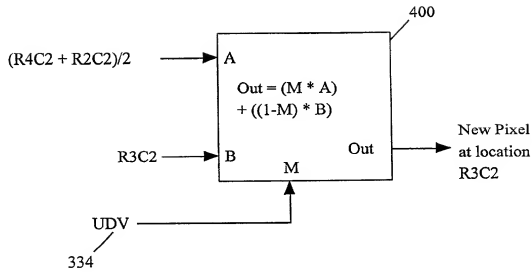


Figure 17

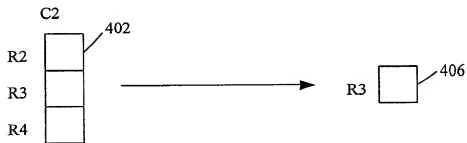


Figure 18

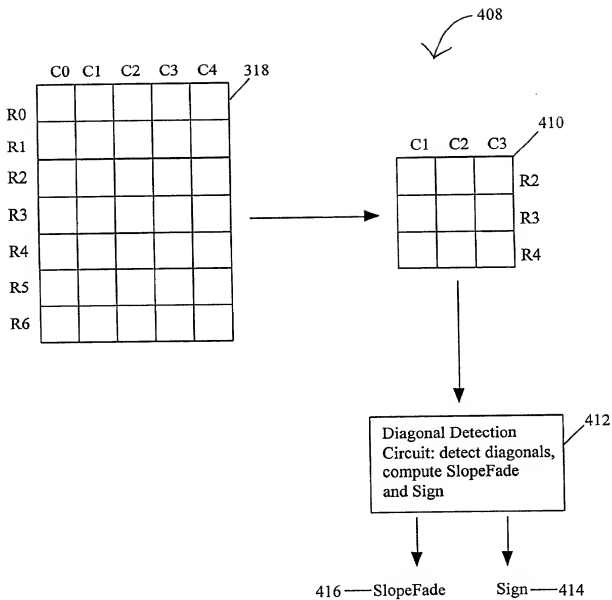


Figure 19

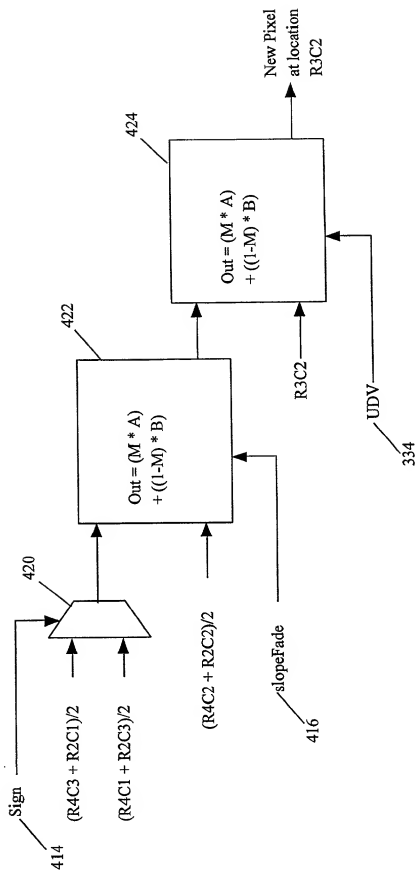


Figure 20

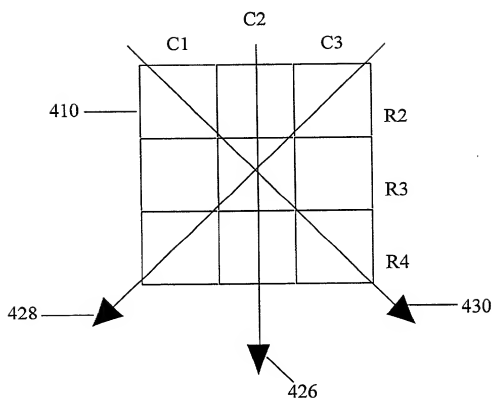
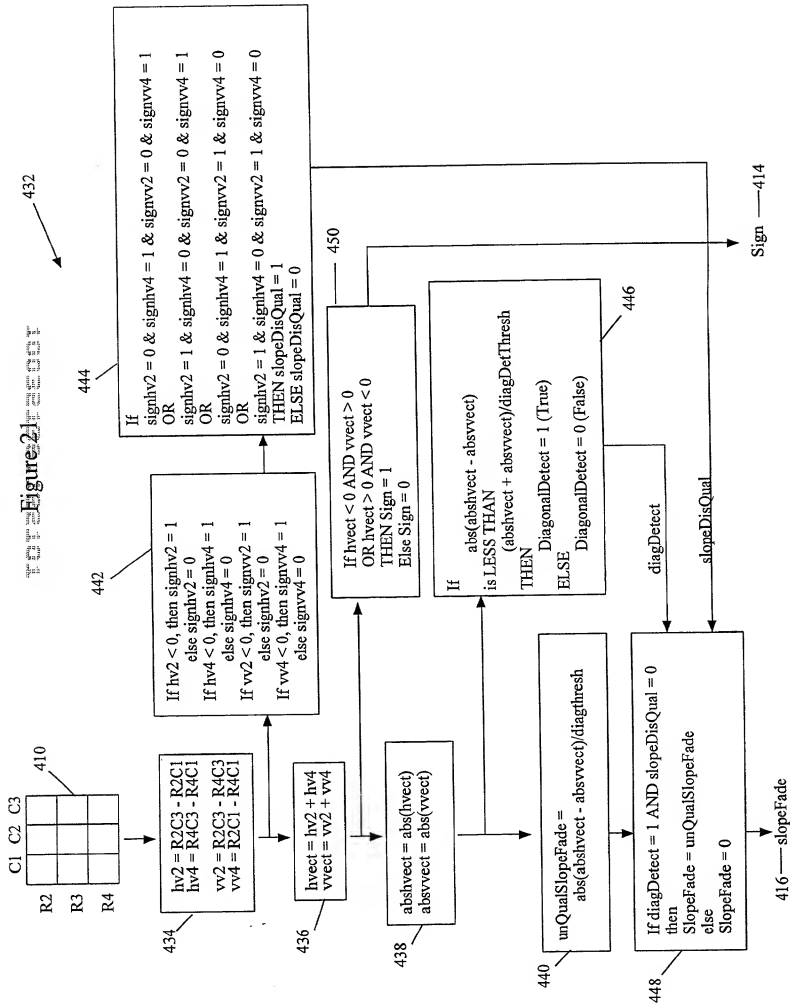




Figure 21



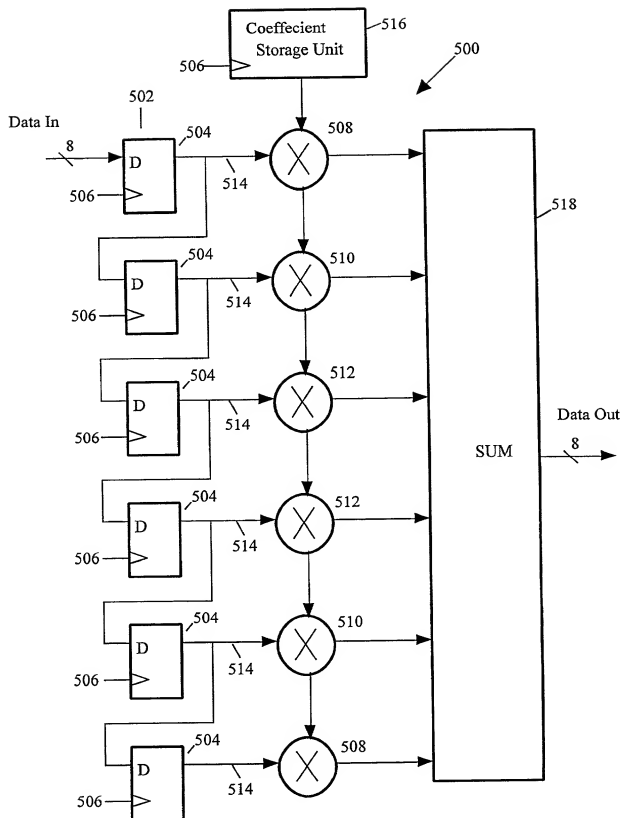


Figure 22

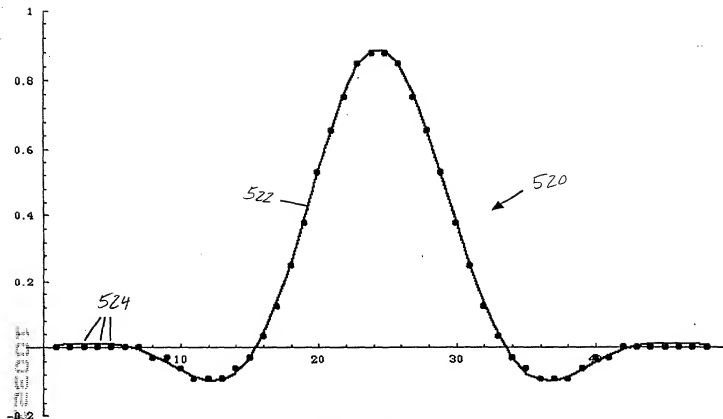


FIG. 23

set(1)	c(1), c(9), c(17), c(25), c(33), c(41)
set(2)	c(2), c(10), c(18), c(26), c(34), c(42)
set(3)	c(3), c(11), c(19), c(27), c(35), c(43)
set(4)	c(4), c(12), c(20), c(28), c(36), c(44)
set(5)	c(5), c(13), c(21), c(29), c(37), c(45)
set(6)	c(6), c(14), c(22), c(30), c(38), c(46)
set(7)	c(7), c(15), c(23), c(31), c(39), c(47)
set(8)	c(8), c(16), c(24), c(32), c(40), c(48)

FIG. 24

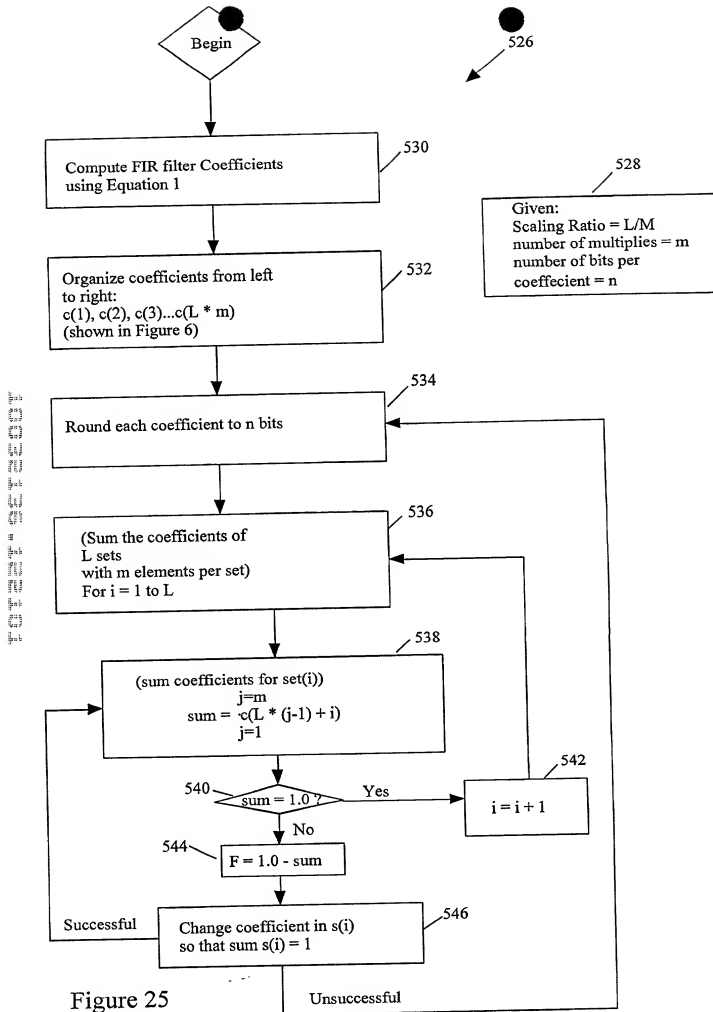


Figure 25

Change coefficient in  $s(i)$   
so that  $\text{sum } s(i) = 1$

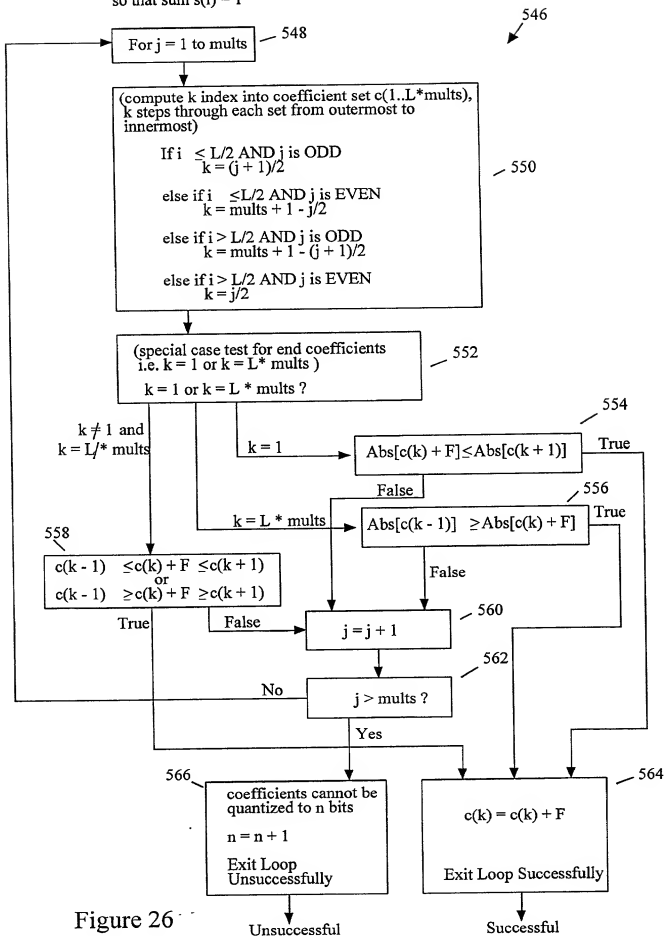


Figure 26

600

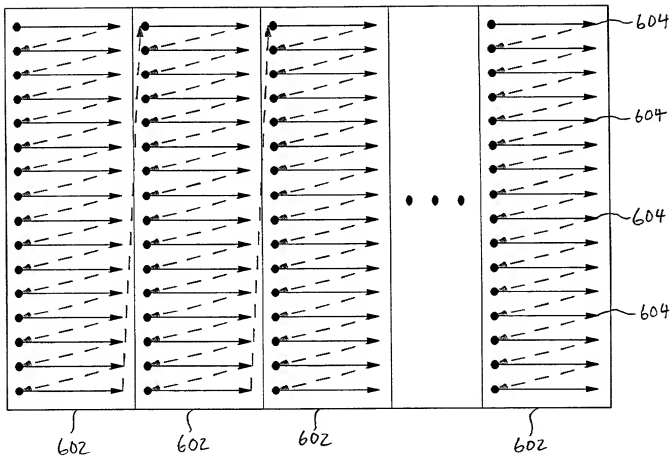
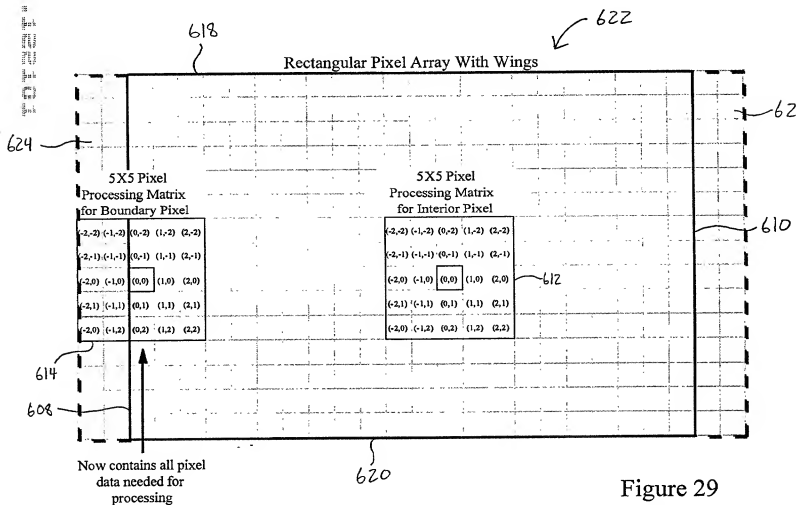
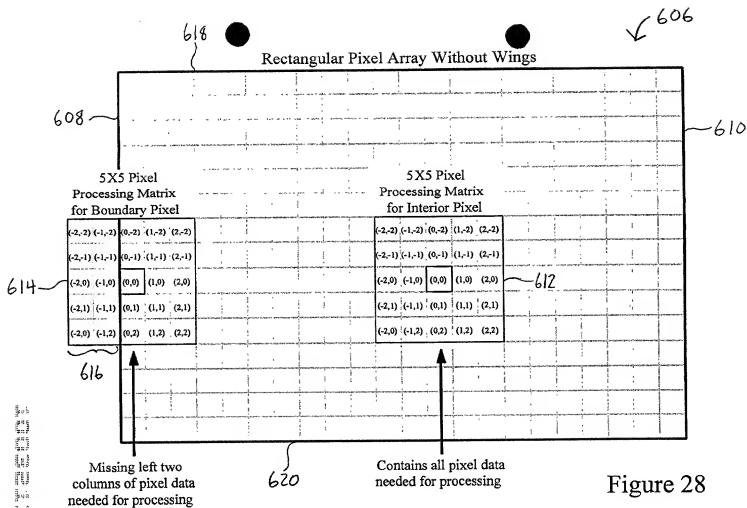


Figure 27



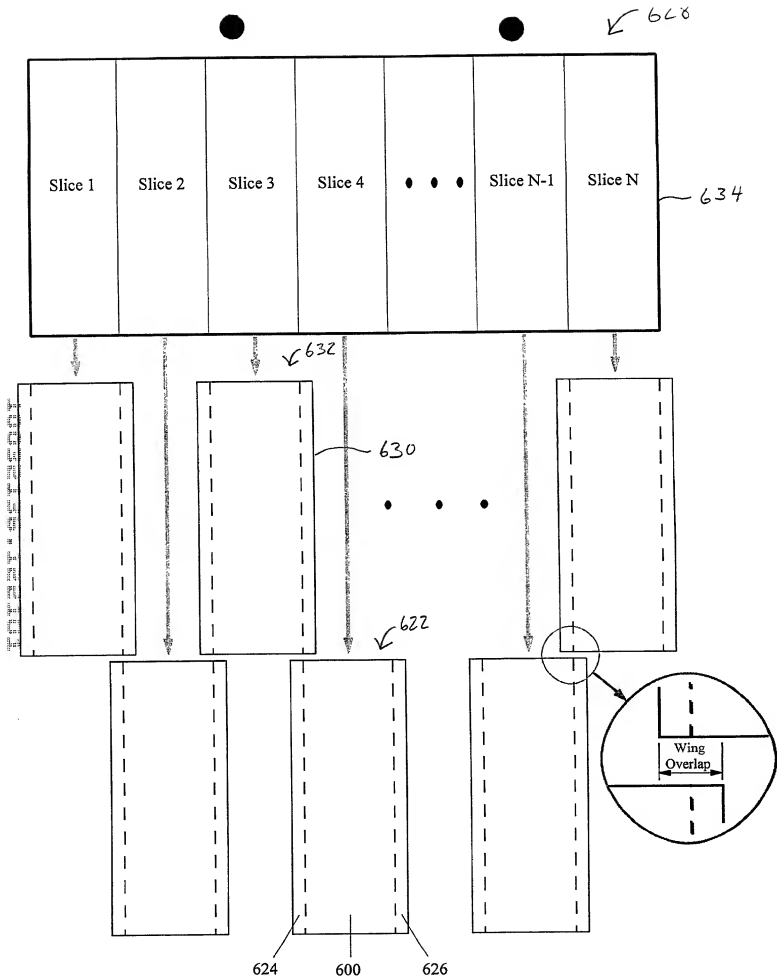


Figure 30



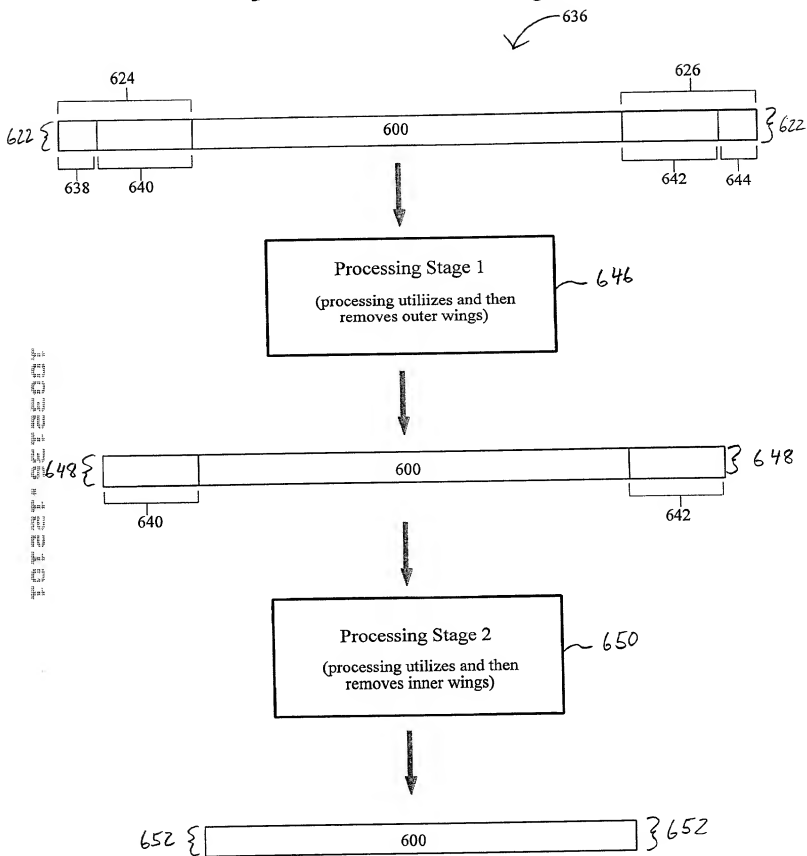


Figure 31

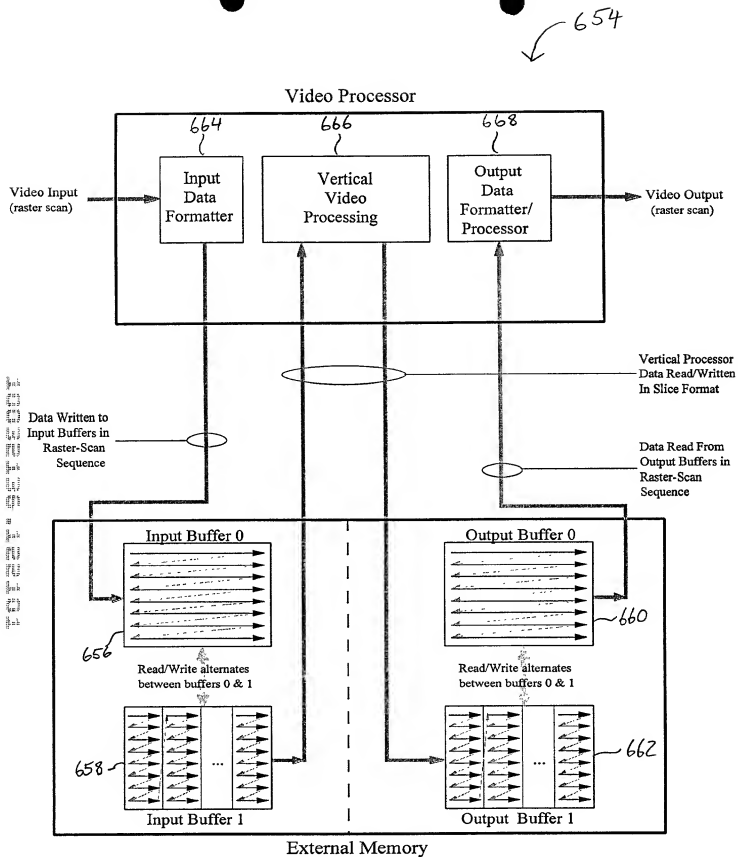


Figure 32

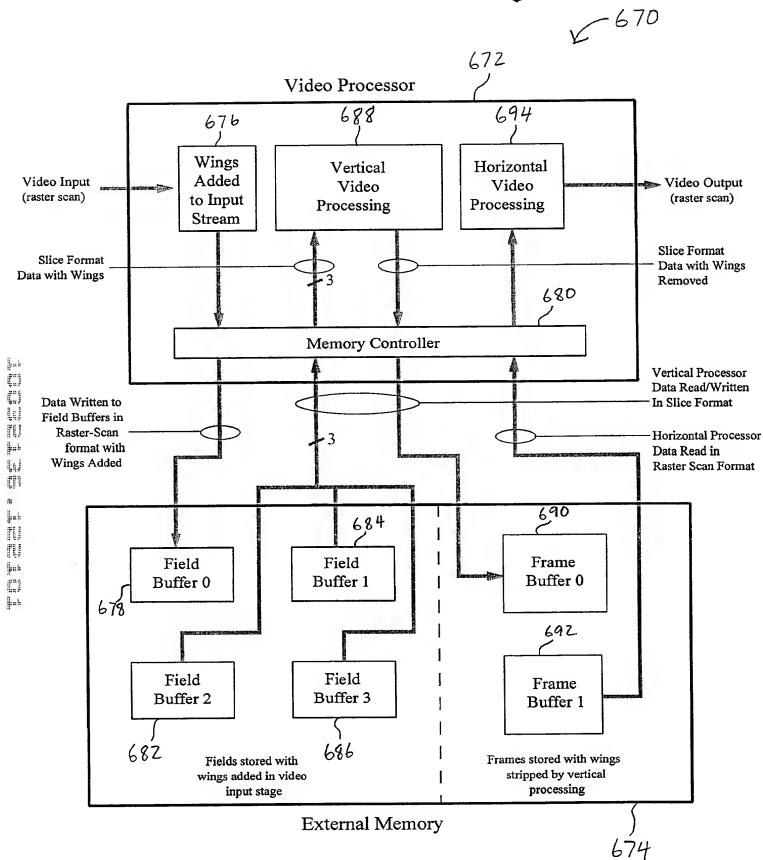


Figure 33

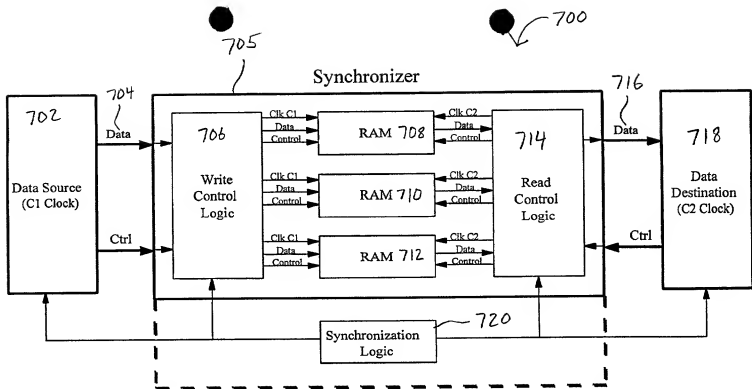


Figure 34

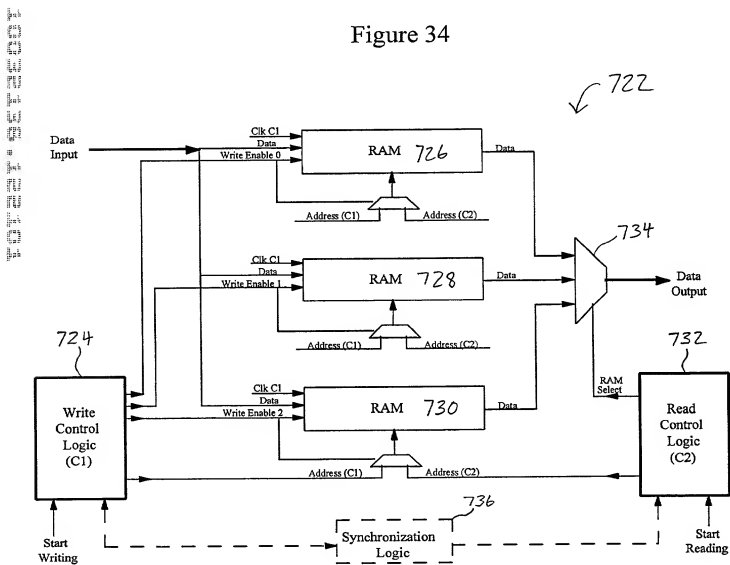
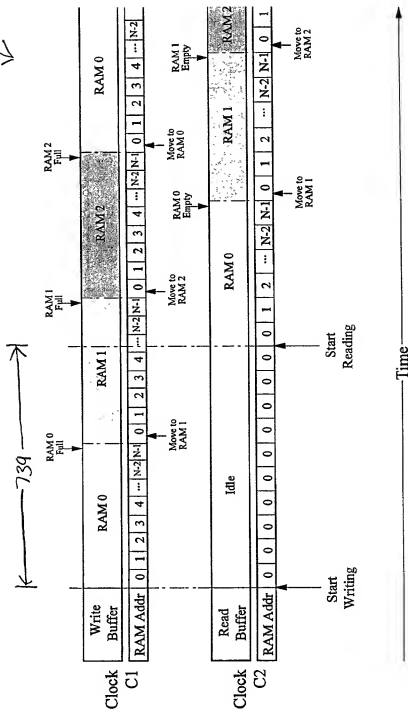
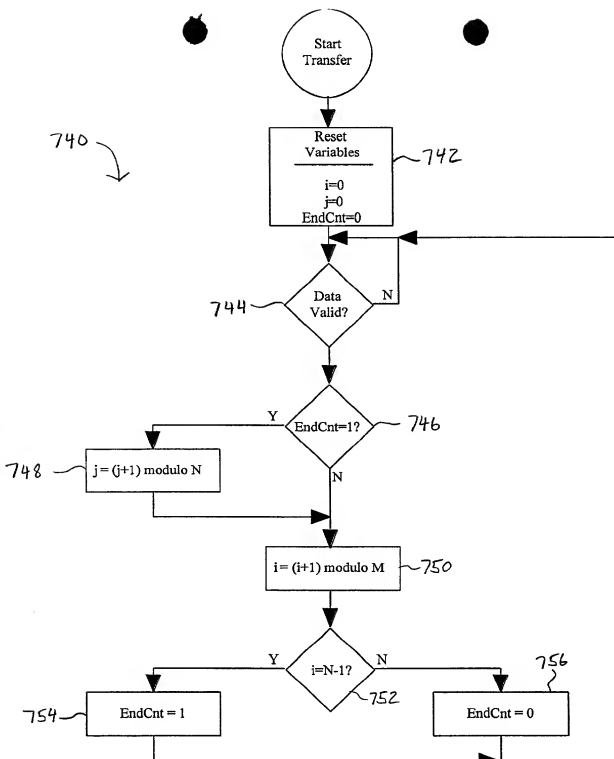


Figure 35



Note: Each RAM Has N Addressable Locations

Figure 36



#### NOTES:

1. "i" is the RAM Address
2. "j" denotes the selected RAM module  
(the address MUX control and RAM write enable)
3. "EndCnt" indicates that the RAM Address points  
to the last location in a RAM module
4. "M" is the number of addressable location in a  
RAM module
5. "N" is the number of RAM modules

Figure 37

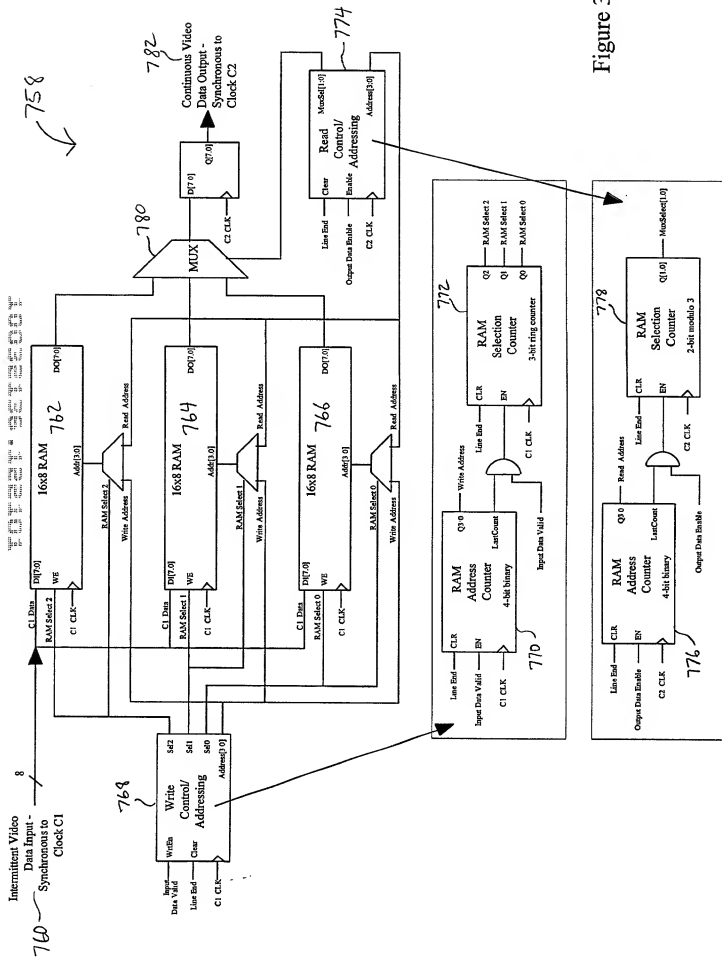


Figure 38